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Implementation Of Content Addressable Memory To Improve Search Speed Using Dual Matched Line

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Abstract - The Content addressable memory which is known as CAM operates faster as it obtains the output in one clock cycle. To improve the search speed and reduce power consumption of Content addressable memory, by combining charge sharing and segmentation techniques. To obtain high search speed a CAM compares its stored word simultaneously and identifies the location of the matched data. In conventional CAM design single matched line is used where as in extended CAM design Dual matched line is used. The simulation results of both single matched line and Dual matched line are compared. A CAM is a memory that implements lookup table function in a single clock cycle using dedicated comparison circuitry. CAMs are especially popular in network routers for packet forwarding and packet classification, but they are also beneficial in a variety of other applications that require high – speed table lookup. The main CAM – design challenge is to reduce power consumption associated with the large amount of parallel active circuitry, without sacrificing speed or memory density.

***Key Words*:** CAM, matched data, Dual matched line, clock cycle lookup table.

1. INTRODUCTION

Content addressable memory (CAM) is a special type of computer memory used in certain very high speed searching applications. It is also known as associative memory, associative storage, or associative array, although the last term is more often used for a programming data structure. It compares input search data (tag) against a table of stored data, and returns the address of matching data (or in the case of associative memory, the matching data). Several custom computers were built to implement CAM and designated associative computers.

Content addressable memories (CAM) are widely used in digital systems, like router, cryptography etc. With the advent technology , large Cams can be embedded into system-on-chips (SOCs) performance and power consumption of CAMs can significantly be improved however, testing embedded CAMs is difficult than RAM testing, since CAM cell structure is more complicated.

Most memory devices store and retrieve data by accessing its specific memory locations. But Content – addressable memory (CAM) is a type of memory in which it can be accessed by using its content instead of using memory locations. As a result, the time required to find an item stored in memory can be reduced. Hence, content addressable memory (CAM) is one such memory that is fast and intuitive. The fast operation of CAM comes at the cost of increased power consumption and area.

The fast operation of CAM is due to the parallel searching operation of contents with all the stored contents in the memory in a single clock cycle. That is, CAM simultaneously searches the input word with all the contents stored in the memory. But, this results in the high power dissipation in the CAM. Hence, due to parallel searching operation in CAM, power consumption is a major concern while designing CAM. There are various types of applications in which high speed of operation is required.

CAMs can be used in these types of applications of CAM is that; it is used in high speed network routers for packet classification and packet forwarding. As CAM application grows, there is a demand of large CAM sizes which worsens the problem of power. So the main challenge is to reduce power consumption in large capacity CAMs without sacrificing its speed. A CAM architecture is proposed in which parity bit is used. This proposed CAM architecture consumes less power and increase the searching speed than the searching speed than the basic CAM

2. MATERIALS AND METHDOLOGY

2.1 CAM cell

Content Addressable Memory is a storage device that stores data in its memory cell like usual memory. But additionally it also has a comparison circuitry which is used to compare search data with the data contents stored in its memory simultaneously. This comparison circuitry in the CAM cell occupies extra area than usual memory cell. Hence there is more dissipation but high speed due to parallel searching operation. Hence a basic CAM cell has two functions

1) Bit storage like usual memory RAM. So this bit storage uses simple SRAM cell which contains two cross coupled inverters forming positive feedback working as a D-Latch.
2) Bit comparison which is equivalent to XNOR logic operation. It is unique in CAM. So, it has three modes of operation: read, write and compare.

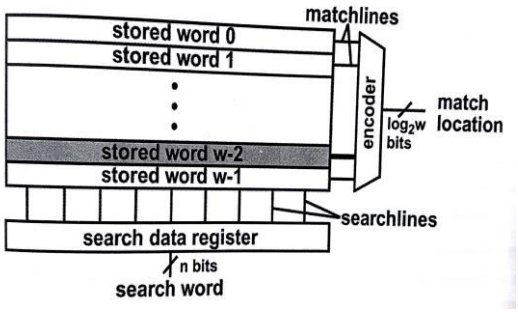


Fig -1: CAM Cell

The conceptual view diagram of CAM is shown in Figure1. It shows that CAM contains m data words in which data is stored. The search word is the n bit input data which is broadcasted onto the search lines to compare it with the table of stored words simultaneously.

There is a match line associated with each word which indicates whether the search data is matched with the stored data or not. If the search data is matched with stored data, it is a match case otherwise mismatch case.

These match lines are fed to an encoder. This encoder generates the binary location corresponding to match line which indicates the match case. If there are more than one match line that indicates the match case then the priority encoder can be used to generate the matched memory location. The priority encoder gives the matching address location corresponding to highest priority match line.

2.2 Typical CAM Architecture

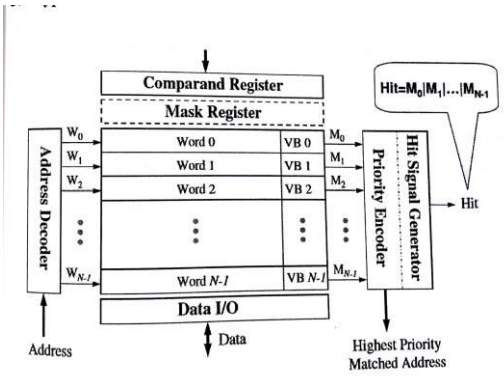


Fig -2: CAM Architecture

Basic Components of CAM architecture are,

Comparand Register: It contains the data to be compared with the content of the memory array.

Mask Register: It is used to mask off portions of the data word which do not participate in the operations.

Memory Array: It provides storage and search medium for data.

Hit Signal Generator/Priority Encoder: It indicates success or Failure of a compare operation.

2.3 Block diagram

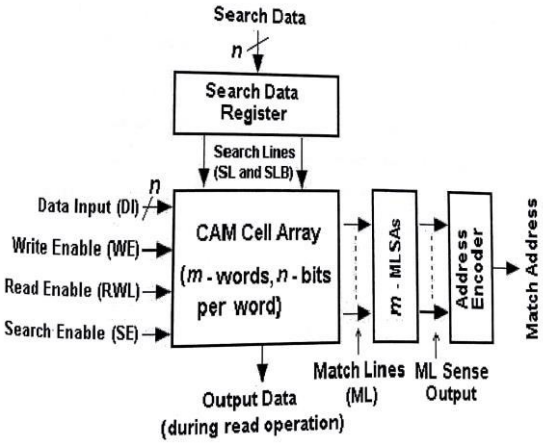


Fig -3: Block diagram of CAM

Figure 3 shows a simplified block diagram of a CAM. The input to the system is the search word that is broadcast onto the search lines to the table of stored data. The number of bits in a CAM word is usually large, with existing implementations ranging from 36 to 144 bits. Atypical CAM employs a table size ranging between a few hundred entries to 32K entries, corresponding to an address space ranging from 7 bits to 15 bits. Each stored word has a match line that indicates whether the search word and stored word are identical (the match case) or are different (a mismatch case, or miss)

The match lines are fed to an encoder that generates a binary match location corresponding to the match line that is in the match state. An encoder is used in systems where only a single match is expected. In CAM applications where more than one word may match, a priority encoder is used instead of a simple encoder. A priority encoder selects the highest priority match in location to map to the match result, with words in lower address locations receiving higher priority.

In addition, there is often a hit signal that flags the case in which there is no matching location in the CAM. The overall function of a CAM is to take a search word and return the matching memory location. One can think of this operation as a fully programmable arbitrary mapping of the large space of the input search word to the smaller space of the output match location.

The operation of a CAM is like that of the tag portion of a fully associative cache. The tag portion of a cache compares its input, which is an address, to all addresses stored in the tag memory. In the case of match, a single match line goes high, indicating the location of a match. Unlike CAMs, caches do not use priority encoders since only a single match occurs; instead, the match line directly activates a read of the data portion of the cache associated with the matching tag. Many circuits are common to both CAMs and caches; however, we focus on large capacity CAMs rather than on fully associative caches, which target smaller capacity and higher speed.

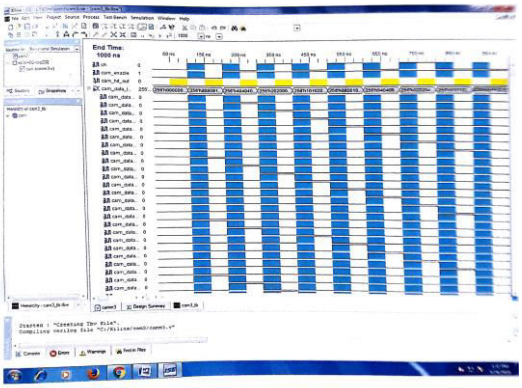
2.4 Software requirement

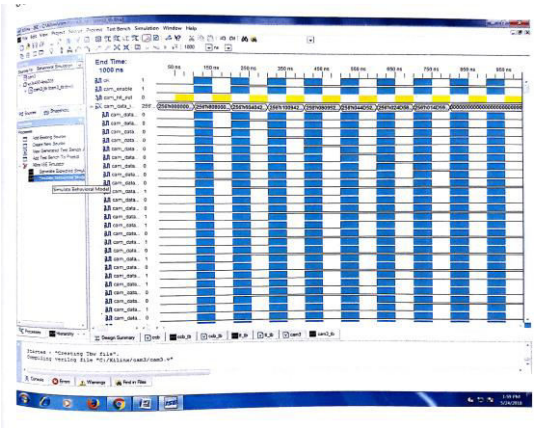
Xilinx ISE is a software tool produced by Xilinx for synthesis and analysis of HDL designs, enabling the developer to synthesize their designs, perform timing analysis, examine RTL diagrams, simulate a design's reaction to different stimuli, and target device with the programmer.

Xilinx tools are a suite of software tools used for the design of digital circuits implemented using Xilinx Field Programmable Logic Device (CPLD). The design procedure consists of design entry, synthesis and implementation of the design, functional simulation and testing and verification. Digital designs can be entered in various ways using the above CAD tools, using a schematic entry tool, using a hardware description language (HDL) – Verilog or VHDL or a combination of both. In this lab we only use the design flow that involves the use of Verilog HDL.

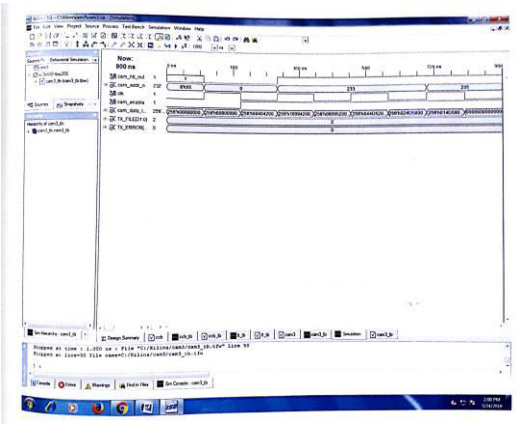
3. RESULTS AND DISCUSSIONS

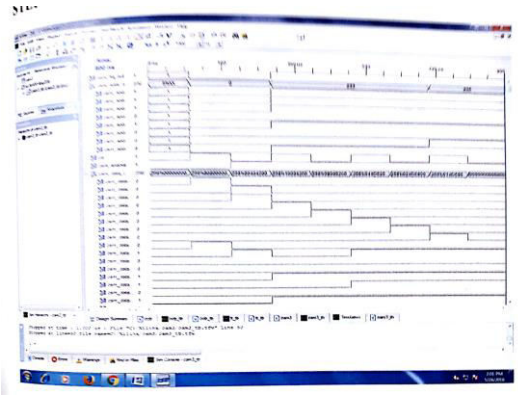
Assign the input clock, enable and data signal. Double click on simulate behavioral Model.



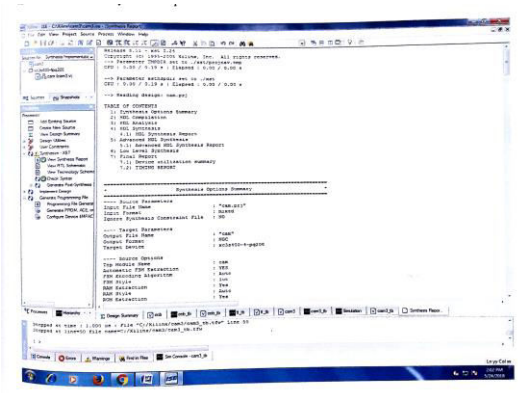


Then the output waveform window showing the simulation result is obtained

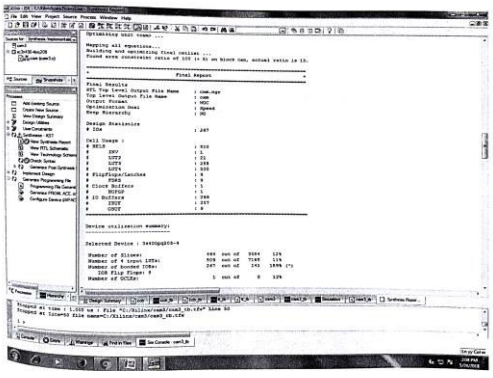




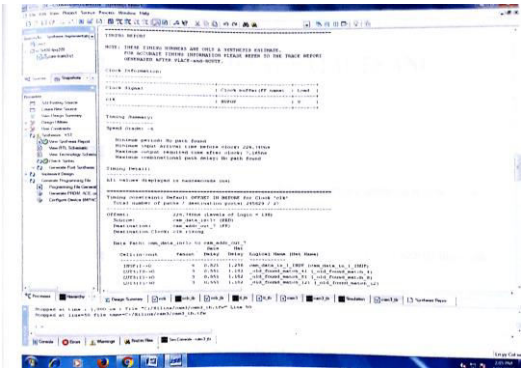
. The synthesis report is generated



Final report is generated which consists of information about Lookup table , clock and I/o Buffers.



The timing report is obtained for Accurate timing information about minimum input arrival time , maximum output required time, fan-out and delay.



4. CONCLUSIONS

In this paper we extend a single matched line CAM with a dual matched line content addressable memory which have various advantages namely power dissipated up to 56.8% and the delay decreased up to 1.43% due to which the search speed of the CAM circuit increased when it is compared with conventional CAM design. So, from this the conclusion obtained is dual matched line is better than single matched line. With an emphasis on high-capacity CAM. At the circuit level, it is reviewed that the two basic CMOS cells, namely the NOR cell and the NAND cells and the cells are combined in a match line structure to from a CAM word.

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